IN THE CLAIMS

1. (Currently amended) A method for phase detection by an exclusive-OR gate in a half-rate phase detector using a clock signal synthesized from an incoming data signal, comprising:

producing delayed versions of the clock signal;

producing delayed versions of the incoming data signal;

combining a first delayed version of the incoming data signal with alternate transitions of a first delayed version of the clock signal to produce first precursor signals;

multiplexing the first precursor signals in response to a second delayed version of the clock signal to produce a multiplexed signal;

providing the multiplexed signal only to an input of the exclusive-OR gate; and

combining the multiplexed signal with a second delayed version of the incoming data signal in the exclusive-OR gate to produce a phase signal indicative of a phase difference between the incoming data signal and the clock signal.

2. (Canceled)

3. (Currently amended) The method of claim ~~2~~ 1, further including:

combining ~~one of~~ the first precursor signals ~~and a second delayed version of the incoming data signal~~ with alternate transitions of the second delayed version of the clock signal to produce second precursor signals; and

combining the second precursor signals to produce a reference signal indicative of a degree of synchronization between an interval in the incoming data signal and a corresponding integration interval.

4. (Original) The method of claim 3 wherein combining the second precursor signals includes the exclusive disjunction of the second precursor signals.

5. (Original) The method of claim 4, further including adjusting a DC voltage level of the reference signal.

6. (Currently amended) A half-rate phase detector for indicating a phase difference between an incoming data signal and a clock signal synthesized from the incoming data signal, comprising:

a first latch circuit for combining a first delayed version of the incoming data signal with alternate transitions of a first delayed version of the clock signal to produce first precursor signals;

a multiplexer connected to the first latch circuit for multiplexing the first precursor signals in response to a second delayed version of the clock signal to produce a multiplexed signal, the multiplexer including an output for providing the multiplexed signal to a single input; ~~and~~

a first logic gate with a first input connected to the multiplexer output and a second input for receiving a second delayed version of the incoming data signal for combining the multiplexed signal with ~~a~~ the second delayed version of the incoming data signal to produce a phase signal indicative of a phase difference between the incoming data signal and the clock signal.

7. (Original) The half-rate phase detector of claim 6 wherein the first logic gate is a first exclusive-OR gate.

8. (Currently amended) The half-rate phase detector of claim 7, further including:

a second latch circuit connected to the first latch circuit for combining ~~one of~~ the first precursor signals ~~and a second delayed version of the incoming data signal~~ with alternate transitions of the second delayed version of the clock signal to produce second precursor signals; and

a second logic gate connected to the second latch circuit for combining the second precursor signals to produce a reference signal indicative of a degree of synchronization between an interval in the incoming data signal and a corresponding integration interval.

9. (Original) The half-rate phase detector of claim 8 wherein the second logic gate is a second exclusive-OR gate.

10. (Original) The half-rate phase detector of claim 9, further including means connected the second exclusive-OR gate for adjusting a DC voltage level of the reference signal.

11. (Currently amended) A half-rate phase detector for detecting a phase difference between a data signal and a clock signal, comprising:

an input for receiving the data signal;

a first latch for sampling a first delayed version of the data signal in response to a first delayed version of the clock signal, the first latch having an output;

a second latch for sampling the first delayed version of the data signal in response to the inverse of the first delayed version of the clock signal, the second latch having an output;

a multiplexer having a first input connected to the output of the first latch, a second input connected to the output of the second latch, a control input for receiving a second delayed version of the clock signal, and an output; and

a first exclusive-OR gate having a first input connected to the output of the multiplexer, a second input for receiving a second delayed version of the data signal, and an output for producing a phase signal representing a phase difference between the data signal and the clock signal;

the multiplexer output being connected only to the first input of the exclusive-OR gate.

12. (Currently amended) The half-rate phase detector of claim 11, further comprising:

a third latch having a data input connected to the output of the first latch, a clock input for receiving the inverse of a second delayed version of the clock signal, and an output;

a fourth latch having a data input ~~for receiving the second delayed version of the data signal~~ connected to the output of the second latch, a clock input for receiving ~~the inverse of~~ the second delayed version of the clock signal, and an output; and

a second exclusive-OR gate having a first input connected to the output of the third latch, a second input connected to the output of the fourth latch, and an output for producing a reference signal indicative of a degree of synchronization between an interval in the data signal and a corresponding integration interval.

13. (Original) The half-rate phase detector of claim 12, further comprising a DC offset input in the second exclusive-OR gate.

14. (Original) The half-rate phase detector of claim 13, further comprising:

a latch circuit having an input for receiving the first delayed version of the data signal for decoding data from the data signal in response to a third delayed version of the clock signal and a fourth delayed version of the clock signal.

15. (Original) The half-rate phase detector of claim 14, wherein the latch circuit comprises:

a fifth latch with an input for receiving the first delayed version of the data signal, a clock input for receiving the third delayed version of the clock signal, and an output;

a sixth latch with an input connected to the output of the fifth latch, a clock input for receiving the inverse of the fourth delayed version of the clock signal, and an output;

a seventh latch with an input connected to the output of the sixth latch, a clock input for receiving the fourth delayed version of the clock signal, and an output for providing a decoded data signal in a first polarity;

an eighth latch with an input for receiving the first delayed version of the data signal, a clock input for receiving the inverse of the third delayed version of the clock signal, and an output; and

a ninth latch with an input connected to the output of the eighth latch, a clock input for receiving the fourth delayed version of the clock signal, and an output for providing a decoded data signal in a second polarity.

16. (Currently amended) A method executable by a half-rate phase detector for detecting a phase difference between a data signal and a clock signal, the method comprising:

receiving the data signal;

sampling a first delayed version of the data signal in a first latch in response to a first delayed version of the clock signal, the first latch having an output;

sampling the first delayed version of the data signal in a second latch in response to the inverse of the first delayed version of the clock signal, the second latch having an output;

producing a ~~precursor~~ multiplexed signal by multiplexing the outputs of the first latch and the second latch in response to a second delayed version of the clock signal;

providing the multiplexed signal to only a single input; and

combining the ~~precursor~~ multiplexed signal provided to only a single input with a second delayed version of the data signal in a first exclusive-OR gate to produce a phase signal representing a phase difference between the data signal and the clock signal.

17. (Currently amended) The method of claim 16, further comprising:

sampling the output of the first latch in a third latch having a data input connected to the output of the first latch, a clock input for receiving the inverse of a second delayed version of the clock signal, and an output;

sampling the output of the second latch in a fourth latch having a data input ~~for receiving the second delayed version of the data signal~~ connected to the output of the second latch, a clock input for receiving ~~the inverse of~~ the second delayed version of the clock signal, and an output; and

combining the output of the third latch with the output of the fourth latch in a second exclusive-OR gate to produce a reference signal indicative of a degree of synchronization between an interval in the data signal and a corresponding integration interval.

18. (Currently amended) The method of claim ~~16~~ 17, further comprising adjusting the DC voltage level of the reference signal by applying a DC offset input in the second exclusive-OR gate.

19. (Original) The half-rate phase detector of claim 18, further comprising:

decoding data from the data signal in a latch circuit in response to a third delayed version of the clock signal and a fourth delayed version of the clock signal.

20. (Original) The half-rate phase detector of claim 19, wherein decoding data comprises:

sampling the first delayed version of the data signal in a fifth latch in response to third delayed version of the clock signal;

sampling an output of the fifth latch in a sixth latch in response to the inverse of the fourth delayed version of the clock signal;

sampling an output of the sixth latch in a seventh latch in response to the fourth delayed version of the clock signal to provide a decoded data signal in a first polarity;

sampling the first delayed version of the data signal in an eighth latch in response to the inverse of the third delayed version of the clock signal; and

sampling an output of the eighth latch in a ninth latch in response to the fourth delayed version of the clock signal to provide a decoded data signal in a second polarity.